APPENDIX A

1 (Cancelled).

2 (New). A method for providing single-ended signaling in a memory controller comprising the steps of:

disabling a differential drive circuit coupled to a first signal line and a second signal line in the memory controller;

controlling a first single-ended drive circuit coupled to the first signal line in the memory controller so as to provide a first single-ended signal on the first signal line; and

controlling a second single-ended drive circuit coupled to the second signal line in the memory controller so as to provide a second single-ended signal on the second signal line.

3 (New). The method of claim 2, wherein the differential drive circuit is disabled so as to provide high impedances on the first signal line and the second signal line.

4 (New). The method of claim 3, wherein the high impedances on the first signal line and the second signal line effectively isolate the first signal line and the second signal line from an influence of any voltage reference through the differential drive circuit.

5 (New). A method for providing single-ended signaling in a memory controller comprising the steps of:

disabling a differential drive circuit coupled to a first signal line and a second signal line in the memory controller;

controlling a first single-ended drive circuit coupled to the first signal line in the memory controller so as to provide a first single-ended signal on the first signal line; and

controlling a second single-ended drive circuit coupled to the second signal line in the memory controller so as to enable a termination of the second signal line.

6 (New). The method of claim 5, wherein the differential drive circuit is disabled so as to provide high impedances on the first signal line and the second signal line.

7 (New). The method of claim 6, wherein the high impedances on the first signal line and the second signal line effectively isolate the first signal line and the second signal line from an influence of any voltage reference through the differential drive circuit.

8 (New). The method of claim 5, wherein the termination of the second signal line is a single reference termination of the second signal line.

9 (New). The method of claim 5, wherein the termination of the second signal line is a double reference termination of the second signal line.

10 (New). A method for providing single-ended signaling in a memory controller comprising the steps of:

disabling a differential drive circuit coupled to a first signal line and a second signal line in the memory controller;

controlling a first single-ended drive circuit coupled to the first signal line in the memory controller so as to provide a first single-ended signal on the first signal line; and

controlling a second single-ended drive circuit coupled to the second signal line in the memory controller so as to provide a high impedance on the second signal line.

11 (New). The method of claim 10, wherein the differential drive circuit is disabled so as to provide high impedances on the first signal line and the second signal line.

12 (New). The method of claim 11, wherein the high impedances on the first signal line and the second signal line effectively isolate the first signal line and the second signal line from an influence of any voltage reference through the differential drive circuit.

13 (New). The method of claim 10, wherein the high impedance on the second signal line effectively isolates the second signal line from an influence of any voltage reference through the second single-ended drive circuit.

14 (New). A method for terminating signal lines in a memory controller comprising the steps of:

disabling a differential drive circuit coupled to a first signal line and a second signal line in the memory controller;

controlling a first single-ended drive circuit coupled to the first signal line in the memory controller so as to enable a termination of the first signal line; and

controlling a second single-ended drive circuit coupled to the second signal line in the memory controller so as to enable a termination of the second signal line.

15 (New). The method of claim 14, wherein the differential drive circuit is disabled so as to provide high impedances on the first signal line and the second signal line.

16 (New). The method of claim 15, wherein the high impedances on the first signal line and the second signal line effectively isolate the first signal line and the second signal line from an influence of any voltage reference through the differential drive circuit.

17 (New). The method of claim 14, wherein the termination of the first signal line is a single reference termination of the first signal line.

18 (New). The method of claim 14, wherein the termination of the first signal line is a double reference termination of the first signal line.

19 (New). The method of claim 14, wherein the termination of the second signal line is a single reference termination of the second signal line.

20 (New). The method of claim 14, wherein the termination of the second signal line is a double reference termination of the second signal line.

21 (New). A method for terminating and isolating signal lines in a memory controller comprising the steps of:

disabling a differential drive circuit coupled to a first signal line and a second signal line in the memory controller;

controlling a first single-ended drive circuit coupled to the first signal line in the memory controller so as to enable a termination of the first signal line; and

controlling a second single-ended drive circuit coupled to the second signal line in the memory controller so as to provide a high impedance on the second signal line.

22 (New). The method of claim 21, wherein the differential drive circuit is disabled so as to provide high impedances on the first signal line and the second signal line.

23 (New). The method of claim 22, wherein the high impedances on the first signal line and the second signal line effectively isolate the first signal line and the second signal line from an

influence of any voltage reference through the differential drive circuit.

24 (New). The method of claim 21, wherein the termination of the first signal line is a single reference termination of the first signal line.

25 (New). The method of claim 21, wherein the termination of the first signal line is a double reference termination of the first signal line.

26 (New). The method of claim 21, wherein the high impedance on the second signal line effectively isolates the second signal line from an influence of any voltage reference through the second single-ended drive circuit.

27 (New). A method for isolating a memory controller comprising the steps of:

disabling a differential drive circuit coupled to a first signal line and a second signal line in the memory controller;

controlling a first single-ended drive circuit coupled to the first signal line in the memory controller so as to provide a high impedance on the first signal line; and

controlling a second single-ended drive circuit coupled to the second signal line in the memory controller so as to provide a high impedance on the second signal line.

28 (New). The method of claim 27, wherein the differential drive circuit is disabled so as to provide high impedances on the first signal line and the second signal line.

29 (New). The method of claim 28, wherein the high impedances on the first signal line and the second signal line effectively isolate the first signal line and the second signal line from an influence of any voltage reference through the differential drive circuit.

30 (New). The method of claim 27, wherein the high impedance on the first signal line effectively isolates the first signal line from an influence of any voltage reference through the first single-ended drive circuit.

31 (New). The method of claim 27, wherein the high impedance on the second signal line effectively isolates the second signal line from an influence of any voltage reference through the second single-ended drive circuit.

32 (New). A method for providing differential signaling in a memory controller comprising the steps of:

controlling a first single-ended drive circuit coupled to a first signal line in the memory controller so as to enable a termination of the first signal line;

controlling a second single-ended drive circuit coupled to a second signal line in the memory controller so as to enable a termination of the second signal line; and

controlling a differential drive circuit coupled to the first signal line and the second signal line in the memory controller so as to provide a differential signal across the first signal line and the second signal line.

33 (New). The method of claim 32, wherein the termination of the first signal line is a single reference termination of the first signal line.

34 (New). The method of claim 32, wherein the termination of the first signal line is a double reference termination of the first signal line.

35 (New). The method of claim 32, wherein the termination of the second signal line is a single reference termination of the second signal line.

36 (New). The method of claim 32, wherein the termination of the second signal line is a double reference termination of the second signal line.

37 (New). A memory controller comprising:

a differential drive circuit coupled to a first signal line and a second signal line in the memory controller, and configured to provide a differential signal across the first signal line and the second signal line when enabled;

a first single-ended drive circuit coupled to the first signal line in the memory controller, and configured to provide a first single-ended signal on the first signal line, provide a high impedance on the first signal line, or enable a termination of the first signal line; and

a second single-ended drive circuit coupled to the second signal line in the memory controller, and configured to provide a second single-ended signal on the second signal line, provide a high impedance on the second signal line, or enable a termination of the second signal line.

38 (New). The memory controller of claim 37, wherein the termination of the first signal line is a single reference termination of the first signal line.

39 (New). The memory controller of claim 37, wherein the termination of the first signal line is a double reference termination of the first signal line.

40 (New). The memory controller of claim 37, wherein the high impedance on the first signal line effectively isolates the first signal line from an influence of any voltage reference through the first single-ended drive circuit.

41 (New). The memory controller of claim 37, wherein the termination of the second signal line is a single reference termination of the second signal line.

42 (New). The memory controller of claim 37, wherein the termination of the second signal line is a double reference termination of the second signal line.

43 (New). The memory controller of claim 37, wherein the high impedance on the second signal line effectively isolates the second signal line from an influence of any voltage reference through the second single-ended drive circuit.

44 (New). The memory controller of claim 37, wherein the differential drive circuit is further configured to provide high impedances on the first signal line and the second signal line when disabled.

45 (New). The memory controller of claim 44, wherein the high impedances on the first signal line and the second signal line provided by the differential drive circuit effectively isolate the first signal line and the second signal line from an influence of any voltage reference through the differential drive circuit.